UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/730,039	12/05/2000	Moataz A. Mohamed	00CON102P	6842

25700 7590 11/05/2003

FARJAMI & FARJAMI LLP
16148 SAND CANYON
IRVINE, CA 92618

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	6

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/730,039	MOHAMED ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2000 and 26 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 February 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-28 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Drawings as received on 21 February 2001; IDS as received on 15 April 2002; and Change of Address as received on 26 September 2002

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 4A, element 412 and Figure 4B, element 432. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 7-10, 21-23, and 27-28 rejected under 35 U.S.C. 102(b) as being taught by Keckler et al., U.S. Patent Number 5,574,939 (herein referred to as Keckler).

8. Referring to claim 1, Keckler has taught a processor comprising:

a. A first plurality of threads, each of said first plurality of threads comprising one of a second plurality of processing units (Keckler column 2, lines 3-17 and 22-38; Figure 1; Figure 2; and Figure 3);

b. Each of said first plurality of threads receiving a respective one of a third plurality of issue groups (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; Figure 2; and Figure 3). In regards to Keckler, the "multiple operations to be performed in parallel (Keckler column 1, lines 32-35)" is similar to the issue groups, which are "instructions...which can be executed in the same clock cycle (Applicant's Specification Page 2, lines 12-13)".

c. Wherein each of said respective one of said third plurality of issue groups belongs to a respective one of a fourth plurality of instruction packets (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; Figure 2; and Figure 3);

d. Said processor executing said third plurality of issue groups in a single clock cycle, wherein each of said third plurality of issue groups is executed in a respective one of said second plurality of processing units (Keckler column 3, lines 41-61 and Figure 1).

9. Referring to claims 2 and 22, Keckler has taught wherein each of said first, second, third, and fourth pluralities is equal to two (Keckler column 13, line 64 to column 14, line 2). In regards to Keckler, Keckler refers to multiple threads, instructions, issue groups, and execution units as cited above. Since "multiple" means more than one, it includes two.

10. Referring to claims 3 and 23, Keckler has taught wherein each of said fourth/first plurality of instruction packets consists of two issue groups (Keckler column 13, line 64 to column 14, line 2). In regards to Keckler, Keckler refers to multiple threads, instructions, issue groups, and execution units as cited above. Since "multiple" means more than one, it includes two.

11. Referring to claims 7 and 27, Keckler has taught wherein each one of said fourth/first plurality of instruction packets resides in a respective instruction cache and is addressed by a respective program counter (Keckler column 4, lines 28-43; column 5, lines 2-4 and 31-40; column 8, lines 26-44; column 8, line 66 to column 9, line 3; Figure 2; and Figure 3).

12. Referring to claim 8, Keckler has taught wherein each of said first, second, third, and fourth pluralities is equal to four (Keckler column 4, lines 28-43; column 5, lines 31-40; and Figure 2).

13. Referring to claim 9, Keckler has taught a method comprising steps of:

a. Dividing a first instruction packet into a first packet first issue group and a first packet second issue group (Keckler column 2, lines 3-19 and 22-38; Figure 1; Figure 2; and Figure 3);

b. Dividing a second instruction packet into a second packet first issue group and a second packet second issue group (Keckler column 2, lines 3-19 and 22-38; Figure 1; Figure 2; and Figure 3);

c. Providing said first packet first issue group to a first thread having a first thread processing unit, and providing said second packet first issue group to a second thread having a second thread processing unit, whereby said first packet first issue group and said second packet first issue group are executed in a first clock cycle (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3).

14. Referring to claim 10, Keckler has taught providing said first packet second issue group to said first thread having said first thread processing unit, and providing said second packet second issue group to said second thread having said second thread processing unit, whereby said first packet second issue group and said second packet second issue group are executed in a second clock cycle (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3).

15. Referring to claim 21, Keckler has taught a method comprising steps of:

a. Dividing each one of a first plurality of instruction packets into a second plurality of issue groups (Keckler column 2, lines 3-19 and 22-38; Figure 1; Figure 2; and Figure 3);

b. Providing each one of said second plurality of issue groups, in one of a third plurality of clock cycles, to a respective thread having a respective processing unit

(Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3);

c. Executing said first plurality of instruction packets in said third plurality of clock cycles (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3).

16. Referring to claim 28, Keckler has taught wherein said first plurality is equal to four (Keckler column 4, lines 28-43; column 5, lines 31-40; and Figure 2), and wherein each of said second and third pluralities is equal to two (Keckler column 13, line 64 to column 14, line 2). In regards to Keckler, Keckler refers to multiple threads, instructions, issue groups, and execution units as cited above. Since "multiple" means more than one, it includes two.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 4-6, 11-20, and 24-26 rejected under 35 U.S.C. 103(a) as being unpatentable over Keckler et al., U.S. Patent Number 5,574,939 (herein referred to as Keckler) in view of Applicant's admitted prior art (herein referred to as Prior Art).

19. Referring to claim 4, Keckler has not explicitly taught:

a. Wherein each of said plurality of instruction packets is 128/256 bits wide (Applicant's claims 4, 11, 16, and 24);

b. Wherein a first one of said two issue groups is 64/128 bits wide and a second one of said two issue groups is 48/112 bits wide (Applicant's claims 5, 12, 14, 17, 19, and 25); and

c. Wherein a first one of said two issue groups is 48/112 bits wide and a second one of said two issue groups is 64/128 bits wide (Applicant's claims 6, 13, 15, 18, 20, and 26).

20. However, Keckler has taught changes in form and details in the invention would not change the invention (Keckler column 13, line 64 to column 14, line 2). Prior Art has taught:

a. Wherein each of said plurality of instruction packets is 128/256 bits wide (Applicant's claims 4, 11, 16, and 24) (Prior Art page 3, lines 16-17 and page 4, lines 9-10).

b. Wherein a first one of said two issue groups is 64/128 bits wide and a second one of said two issue groups is 48/112 bits wide (Applicant's claims 5, 12, 14, 17, 19, and 25) (Prior Art page 4, line 20 to page 5, line 12).

c. Wherein a first one of said two issue groups is 48/112 bits wide and a second one of said two issue groups is 64/128 bits wide (Applicant's claims 6, 13, 15, 18, 20, and 26) (Prior Art page 4, line 20 to page 5, line 12).

21. In regards to Keckler and Prior Art, the size of the instruction packet and issue groups is not patentable material. See *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) and *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). A person of ordinary skill in the art at the time the invention was made would have recognized the larger bit widths are needed in VLIW instructions to ensure the multiple operations are contained in the VLIW instruction,

thereby allowing multiple instructions to be executed in parallel. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the VLIW bit width of Prior Art in the device of Keckler.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Petit, U.S. Patent Number 4,953,078, has taught a multi-threaded execution device.

b. Moreno, U.S. Patent Number 5,669,001, has taught a VLIW execution device.

c. Ebcioglu et al., U.S. Patent Number 5,721,854, has taught a VLIW execution device.

d. Ishikawa, U.S. Patent Number 5,787,303, has taught a VLIW architecture.

e. O'Connor, U.S. Patent Number 5,848,288, has taught a VLIW device.

f. Pechanek et al., U.S. Patent Number 6,467,036, has taught a VLIW execution device.

g. Alberto Ferreira de Souza and Peter Rounce's "Dynamically Scheduling the Trace Produced During Program Execution into VLIW Instructions" has taught a VLIW machine.

h. Michael Weiss, Zhixi Fang, C. Robert Morgan, and Peter Belmont's "Effective Dynamic Scheduling and Memory Management on Parallel Processing Systems" has taught a device for executing instructions in parallel.

i. Santoshkumar S. Pande, Dharma P. Agrawal, and Jon Mauney's "Palm: An Integrated Parallelism Enhancement Environment with Static-Dynamic Scheduling" has taught a device of executing multiple instructions simultaneously.

j. B. Ramakrishna Rau's "Dynamically Scheduled VLIW Processors" has taught a VLIW processor.

k. Thomas M. Conte and Sumedh W. Sathaye's "Dynamic Rescheduling: A Technique for Object Code Compatibility in VLIW Architectures" has taught a VLIW architecture.

l. Morteza Biglari-Abhari, Kamran Eshraghian, and Michael J. Liebelt's "Improving Binary Compatibility in VLIW Machines through Compiler Assisted Dynamic Rescheduling" has taught a VLIW machine.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

25. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

November 3, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100